REMARKS

By the present amendment and response, independent claims 1 and 12 and dependent claims 8, 10, 16, and 18 have been amended to overcome the Examiner's objections. Claims 1-3 and 5-19 are pending in the present application. Reconsideration and allowance of pending claims 1-3 and 5-19 in view of the following remarks are requested.

The Examiner has objected to claims 1 and 12 due to informalities. Applicant has amended claims 1 and 12 and respectfully submits that the objections to claims 1 and 12 have been traversed.

The Examiner has rejected claims 1-3 and 5-19 under 35 USC §103(a) as being unpatentable over U.S. patent number 5,963,810 to Gardner et al. ("Gardner") and further in view of U.S. patent number 6,124.158 to Dautartas et al. ("Dautartas"). U.S. patent number 5,994,192 to Chun-Yao Chen ("Chen") and "admitted prior art," and U.S. patent number 6.369.430 to Adetutu et al. ("Adetutu"). For the reasons discussed below, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 12, is patentably distinguishable over Gardner, Dautartas, Chen, and Adetutu, singly or in any combination thereof.

The present invention, as defined by amended independent claims 1 and 12, recites, among other things, depositing a first ultra-thin nitride film by atomic layer deposition on a semiconductor substrate that comprises a silicon-on-insulator (SOI) wafer (claim 12), depositing a second ultra-thin nitride film on a high-k material by atom layer

deposition, and depositing a gate material on the second ultra-thin nitride film, "wherein said gate material comprises polysilicon-germanium (poly-SiGe)." As disclosed in the present application, the present invention provides a nitride/high-k material/nitride gate dielectric stack, where each nitride film is deposited by atomic layer deposition to achieve a thickness in a range of 1 to 2 atomic layer(s), and a gate electrode comprising a gate material comprising polysilicon-germanium, which is formed over the gate dielectric stack.

As a result, the present invention achieves a high-k dielectric gate insulator where the first and second nitride films advantageously prevent metal from the high-k material from diffusing into the semiconductor substrate and the polysilicon-germanium gate material, respectively, during subsequent high temperature processes. Thus, the present invention advantageously achieves a high-k dielectric gate insulator having good thermal stability that can be combined with gate material comprising polysilicon-germanium. Additionally, the present invention achieves a high-k dielectric gate insulator that advantageously provides a reduction of direct tunneling current flow in a semiconductor device, such as a MOSFET. Moreover, the present invention advantageously achieves a high-k dielectric gate insulator that can be situated on a semiconductor substrate that can comprise a silicon-on-insulator (SOI) wafer.

In contrast to the present invention as defined by amended independent claims 1 and 12, Gardner, Dautartas, Chen, and Adetutu do not teach, disclose, or suggest depositing a first ultra-thin nitride film by atomic layer deposition on a semiconductor

substrate that comprises a silicon-on-insulator (SOI) wafer (claim 12), by atomic layer deposition, depositing a second ultra-thin nitride film on a high-k material by atom layer deposition, and depositing a gate material on the second ultra-thin nitride film, "wherein said gate material comprises polysilicon-germanium (poly-SiGe)." Gardner specifically discloses forming high permittivity layer 305 over thin nitride layer 303 and forming a nitride capping layer over high permittivity layer 305 prior to forming gate electrode layer 307. See, for example, column 5, lines 52-52, column 6, lines 13-15, and Figure 3C of Gardner.

In Gardner, nitrogen-bearing layers, i.e. thin nitride layer 303 and the nitride capping layer, formed between high permittivity layer 305 and the substrate or gate electrode layer 307 serve to inhibit oxidation of high permittivity layer 305 during subsequent processing. See, for example, Gardner, column 5, lines 13-24. However, Gardner fails to teach, disclose, or suggest forming thin nitride layer 303 and nitride capping layer by using atomic layer deposition.

Additionally, Gardner fails to teach, disclose, or even remotely suggest depositing a first ultra-thin nitride film by atomic layer deposition on a semiconductor substrate that comprises a silicon-on-insulator (SOI) wafer, as specified in amended independent claim 12. In fact, Gardner fails to even mention a silicon-on-insulator (SOI) wafer or provide any motivation for utilizing a semiconductor substrate that comprises a silicon-on-insulator (SOI) wafer. Further, Gardner fails to teach, disclose, or remotely suggest

depositing a gate material comprising polysilicon-germanium on an ultra-thin nitride film by atomic layer deposition.

Dautartas specifically discloses an atomic layer deposition process that is particularly advantageous for deposition of gate dielectric materials, such as aluminum oxide, from organic precursors, particularly trimethyl aluminum, as well as other dielectrics deposited from carbon-containing precursors, such as tantalum oxide from tantalum alcoholate. See, for example, Dautartas, column 3, lines 7-14.

However, Dautartas fails to teach, disclose, or suggest depositing a gate material on an ultra-thin nitride film that has been depositing using an atomic layer deposition (ALD) technique, where the gate material comprises polysilicon-germanium. Furthermore, Dautartas fails to even mention a gate material comprising polysilicon-germanium. Moreover, Dautartas fails to teach, disclose, or suggest depositing an ultra-thin nitride film on a substrate comprising a silicon-on-insulator (SOI) wafer, as specified in amended independent claim 12. In fact, Dautartas fails to even mention a substrate comprising a silicon-on-insulator (SOI) wafer. Thus, Dautartas fails to cure the basic deficiencies of Gardner.

Chen is cited by the Examiner to disclose using a photoresist as part of the patterning process as required in claims 10 and 18-19. However, Chen fails to teach, disclose, or suggest depositing a gate material on an ultra-thin nitride film that has been depositing using an atomic layer deposition (ALD) technique, where the gate material comprises polysilicon-germanium. Additionally, Chen fails to teach, disclose, or suggest

depositing an ultra-thin nitride film on a substrate comprising a silicon-on-insulator (SOI) wafer, as specified in amended independent claim 12. Thus, the combination of Chen and Dautartas fails to cure the basic deficiencies of Gardner.

Adetutu is cited by the Examiner to disclose a substrate comprising a silicon-on-insulator (SOI) wafer, as specified in amended independent claim 12 and dependent claim 2. However, Adetutu does not provide any motivation for depositing an ultra-thin nitride film on a substrate comprising a silicon-on-insulator (SOI) wafer, as specified in amended independent claim 12. Furthermore, Adetutu fails to teach, disclose, or suggest depositing a gate material on an ultra-thin nitride film that has been depositing using an atomic layer deposition (ALD) technique, where the gate material comprises polysilicon-germanium. Thus, the combination of Dautartas, Chen, and Adetutu fails to cure the basic deficiencies of Gardner.

For the foregoing reasons, Applicant respectfully submits that the present invention, as defined by amended independent claims 1 and 12, is not suggested, disclosed, or taught by Gardner, Dautartas, Chen, and Adetutu, singly or in combination. As such, amended independent claims 1 and 12 are patentably distinguishable over Gardner, Dautartas, and Chen. Thus claims 3 and 4-11 depending from amended independent claim 1 and claims 13-19 depending from amended independent claim 12 are, *a fortiori*, also patentably distinguishable over Gardner, Dautartas, Chen, and Adetutu for at least the reasons presented above and also for additional limitations contained in each dependent claim.

Based on the foregoing reasons, the present invention, as defined by amended independent claims 1 and 12, and claims depending therefrom, is patentably distinguishable over the art cited by the Examiner. Thus, claims 1-3 and 5-19 pending in the present application are patentably distinguishable over the art cited by the Examiner. As such, and for all the foregoing reasons, an early allowance of claims 1-3 and 5-19 pending in the present application is respectfully requested.

Attorney Docket No.: 0180197

Respectfully Submitted,
FARJAMI & FARJAMI LLP

Michael Farjami, Esq.
Reg. No. 38, 135

Date: 6/30/04

FARJAMI & FARJAMI LLP
26522 La Alameda Ave., Suite 360
Mission Viejo, California 92691
Telephone: (949) 282-1000
Facsimile: (949) 282-1002

CERTIFICATE OF FACSIMILE TRANSMISSION
I hereby certify that this correspondence is being filed by facsimile transmission to United States Patent and Trademark Office at facsimile number **703-872-9306** on the date stated below. The facsimile transmission report indicated that the facsimile transmission was successful.

Date of Facsimile: 6/30/2004

LESLEY L. LAM
Name of Person Performing Facsimile Transmission

Signature 6/30/04
Date

CERTIFICATE OF MAILING
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

Date of Deposit: _____

Name of Person Mailing Paper and/or Fee

Signature Date